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Computer, Volume: 25 Issue: 5, May 1992

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52 Hierarchical topological sorting of apparent loops via partitioning

Beetem, J.F.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, Volume: 11 Issue: 5, May 1992

Page(s): 607 -619

[\[Abstract\]](#) [\[PDF Full-Text \(872 KB\)\]](#) **IEEE JNL**

53 Combined hardware selection and pipelining in high-performance data-path design

Note, S.; Catthoor, F.; Goossens, G.; De Man, H.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, Volume: 11 Issue: 4, April 1992

Page(s): 413 -423

[\[Abstract\]](#) [\[PDF Full-Text \(1188 KB\)\]](#) **IEEE JNL**

54 Autonomous time synchronization among radio ports in wireless personal communications

Chuang, J.C.-I.;

Vehicular Technology Conference, 1993 IEEE 43rd, 18-20 May 1993

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[\[Abstract\]](#) [\[PDF Full-Text \(524 KB\)\]](#) **IEEE CNF**

55 Topological design of clock distribution networks based on non-zero clock skew specifications

Neves, J.L.; Friedman, E.G.;

Circuits and Systems, 1993., Proceedings of the 36th Midwest Symposium on , 16-18 Aug. 1993

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[\[Abstract\]](#) [\[PDF Full-Text \(420 KB\)\]](#) **IEEE CNF**

56 A high performance fine-grained approach to SRAM based FPGAs

Zlotnick, F.; Butler, P.; Wanhao Li; Dandas Tang;

WESCON/'93. Conference Record, , 28-30 Sept. 1993

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[\[Abstract\]](#) [\[PDF Full-Text \(324 KB\)\]](#) **IEEE CNF**

57 Modelling aspects of system level design

Rammig, F.J.;

Design Automation Conference, 1993, with EURO-VHDL '93. Proceedings

EURO-DAC '93. European , 20-24 Sept. 1993

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[\[Abstract\]](#) [\[PDF Full-Text \(496 KB\)\]](#) **IEEE CNF**

58 Interface specification and synthesis for VHDL processes

Gutberlet, P.; Rosenstiel, W.;

Design Automation Conference, 1993, with EURO-VHDL '93. Proceedings

EURO-DAC '93. European , 20-24 Sept. 1993

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[\[Abstract\]](#) [\[PDF Full-Text \(576 KB\)\]](#) **IEEE CNF**

59 A cell-based datapath synthesizer for ASICs

Ginetti, A.; Mahmood, M.; Sharma, B.;

ASIC Conference and Exhibit, 1993. Proceedings., Sixth Annual IEEE

International , 27 Sept.-1 Oct. 1993

Page(s): 416 -419

[\[Abstract\]](#) [\[PDF Full-Text \(252 KB\)\]](#) **IEEE CNF**

60 A specification driven hierarchical test methodology

Sathianathan, R.; Smith, D.;

ASIC Conference and Exhibit, 1993. Proceedings., Sixth Annual IEEE

International , 27 Sept.-1 Oct. 1993

Page(s): 54 -57

[\[Abstract\]](#) [\[PDF Full-Text \(328 KB\)\]](#) **IEEE CNF**

61 Reducing the physical design cycle by means of topological placement with hard timing restraints

Freier, B.E.;

Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium on , 3-6 May 1993

Page(s): 2063 -2066 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(252 KB\)\]](#) **IEEE CNF**

62 A new accurate and hierarchical timing analysis approach

Blaquiere, Y.; Dagenais, M.; Savaria, Y.;

Design Automation, 1993, with the European Event in ASIC Design. Proceedings. [4th] European Conference on , 22-25 Feb. 1993

Page(s): 449 -454

[\[Abstract\]](#) [\[PDF Full-Text \(504 KB\)\]](#) **IEEE CNF**

63 Timing and chunking in processing temporal order

Wang, D.; Arbib, M.A.;

Systems, Man and Cybernetics, IEEE Transactions on , Volume: 23 Issue: 4 , July-Aug. 1993

Page(s): 993 -1009

[\[Abstract\]](#) [\[PDF Full-Text \(1780 KB\)\]](#) **IEEE JNL**

64 Adaptive synchronization for continuous media storage in a multimedia communication system

Rothlisberger, U.;

Multimedia Communications, 1994. MULTIMEDIA '94., 5th IEEE COMSOC International Workshop on , 16-19 May 1994

Page(s): 7/3/1 -7/3/3

[\[Abstract\]](#) [\[PDF Full-Text \(312 KB\)\]](#) **IEEE CNF**

65 Timing modeling of datapath layout for synthesis

Sharma, B.; Mahmood, M.; Ginetti, A.;

Verilog HDL Conference, 1994., International , 14-16 March 1994

Page(s): 80 -84

[\[Abstract\]](#) [\[PDF Full-Text \(344 KB\)\]](#) **IEEE CNF**

66 A purely behavioral data structure for accurate high level timing simulation of synchronous designs

Arnold, M.G.; Bailey, T.A.; Cowles, J.R.; Cupal, J.J.; Wallace, A.W.;

Verilog HDL Conference, 1994., International , 14-16 March 1994

Page(s): 101 -107

[\[Abstract\]](#) [\[PDF Full-Text \(448 KB\)\]](#) **IEEE CNF**

67 Visual language for behavioral specifications of reactive systems

Chau, H.L.; Chan, G.K.;

Computer Languages, 1994., Proceedings of the 1994 International Conference on , 16-19 May 1994

Page(s): 200 -210

[\[Abstract\]](#) [\[PDF Full-Text \(680 KB\)\]](#) **IEEE CNF**

68 An hierarchical approach to clock routing in high performance systems

Khan, W.; Madhwapathy, S.; Sherwani, N.;

Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International Symposium on , Volume: 1 , 30 May-2 June 1994

Page(s): 467 -470 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(336 KB\)\]](#) **IEEE CNF**

69 Hierarchical mixed-level simulation of VHDL descriptions

Karnik, T.; Saab, D.G.; Kang, S.M.; Lee, Y.K.; Kim, K.H.;

ASIC Conference and Exhibit, 1994. Proceedings., Seventh Annual IEEE International , 19-23 Sept. 1994

Page(s): 170 -173

[\[Abstract\]](#) [\[PDF Full-Text \(276 KB\)\]](#) **IEEE CNF**

70 Digital television

Anastassiou, D.;

Proceedings of the IEEE , Volume: 82 Issue: 4 , April 1994

Page(s): 510 -519

[\[Abstract\]](#) [\[PDF Full-Text \(1104 KB\)\]](#) **IEEE JNL**

71 Fuzzy logic approach to VLSI placement

Kang, E.Q.; Rung-Bin Lin; Shragowitz, E.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 2 Issue: 4 , Dec. 1994

Page(s): 489 -501

[\[Abstract\]](#) [\[PDF Full-Text \(1080 KB\)\]](#) **IEEE JNL**

72 Modechart: a specification language for real-time systems

Jahanian, F.; Mok, A.K.;

Software Engineering, IEEE Transactions on , Volume: 20 Issue: 12 , Dec. 1994

Page(s): 933 -947

[\[Abstract\]](#) [\[PDF Full-Text \(1256 KB\)\]](#) **IEEE JNL**

73 A 150 MHz 8-banks 256 Mb synchronous DRAM with wave pipelining methods

Hoi-Jun Yoo; Kee-Woo Park; Chang-Ho Chung; Seung-Jun Lee; Hak-Jun Oh; Jin-Seung Son; Ki-Hong Park; Ki-Won Kwon; Jeong-Dong Han; Wi-Sik Min; Kye-Hwan Oh;

Solid-State Circuits Conference, 1995. Digest of Technical Papers. 42nd ISSCC, 1995 IEEE International , 15-17 Feb. 1995

Page(s): 250 -251

[\[Abstract\]](#) [\[PDF Full-Text \(868 KB\)\]](#) **IEEE CNF**

74 The VLSI design and implementation of the array processors of a multilayer vision system architecture

Saha, B.; Mertoguno, J.S.; Bourbakis, N.G.;

Application Specific Array Processors, 1995. Proceedings., International Conference on , 24-26 July 1995

Page(s): 125 -128

[\[Abstract\]](#) [\[PDF Full-Text \(212 KB\)\]](#) **IEEE CNF**

75 Hierarchical timing-driven floorplanning and place and route using a timing budgeter

Venkatesh, S.V.;

Custom Integrated Circuits Conference, 1995., Proceedings of the IEEE 1995 , 1-4 May 1995

Page(s): 469 -472

[\[Abstract\]](#) [\[PDF Full-Text \(376 KB\)\]](#) **IEEE CNF**

76 Improved delay root-Nyquist filters for symbol synchronisation in PCS receivers

Sabel, L.P.; Yardim, A.; Cain, G.D.; Laakso, T.L.;

Global Telecommunications Conference, 1995. GLOBECOM '95., IEEE , Volume: 2 , 13-17 Nov. 1995

Page(s): 1302 -1306 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(464 KB\)\]](#) **IEEE CNF**

77 Distributed pipeline scheduling: end-to-end analysis of heterogeneous, multi-resource real-time systems

Chatterjee, S.; Strosnider, J.;

Distributed Computing Systems, 1995., Proceedings of the 15th International Conference on , 30 May-2 June 1995

Page(s): 204 -211

[\[Abstract\]](#) [\[PDF Full-Text \(668 KB\)\]](#) **IEEE CNF**

78 Performability modeling of N version programming technique

Goseva-Popstojanova, K.; Grnarov, A.;
Software Reliability Engineering, 1995. Proceedings., Sixth International Symposium on , 24-27 Oct. 1995
Page(s): 209 -218

[\[Abstract\]](#) [\[PDF Full-Text \(812 KB\)\]](#) **IEEE CNF**

79 Hierarchical timing estimation using a module timing overlapping technique

Kanthamanon, P.; Hellestrand, G.R.; Chan, R.L.K.;
TENCON '95. 1995 IEEE Region 10 International Conference on Microelectronics and VLSI , 6-10 Nov. 1995
Page(s): 147 -150

[\[Abstract\]](#) [\[PDF Full-Text \(340 KB\)\]](#) **IEEE CNF**

80 Hierarchical timing analysis using conditional delays

Yalcin, H.; Hayes, J.P.;
Computer-Aided Design, 1995. ICCAD-95. Digest of Technical Papers., 1995 IEEE/ACM International Conference on , 5-9 Nov. 1995
Page(s): 371 -377

[\[Abstract\]](#) [\[PDF Full-Text \(704 KB\)\]](#) **IEEE CNF**

81 Proceedings the European Design and Test Conference. ED&TC 1995

European Design and Test Conference, 1995. ED&TC 1995, Proceedings. , 6-9 March 1995

[\[Abstract\]](#) [\[PDF Full-Text \(24 KB\)\]](#) **IEEE CNF**

82 Proving testing preorders for process algebra descriptions

Corno, F.; Cusinato, M.; Ferrero, M.; Prinetto, P.;
European Design and Test Conference, 1995. ED&TC 1995, Proceedings. , 6-9 March 1995
Page(s): 333 -337

[\[Abstract\]](#) [\[PDF Full-Text \(380 KB\)\]](#) **IEEE CNF**

83 All-digital multipoint adaptive delay compensation circuit for low skew clock distribution

Grover, W.D.; Brown, J.; Friesen, T.; Marsh, S.;
Electronics Letters , Volume: 31 Issue: 23 , 9 Nov. 1995
Page(s): 1996 -1998

[\[Abstract\]](#) [\[PDF Full-Text \(376 KB\)\]](#) **IEEE JNL**

84 Technique to minimise area overhead for delay-driven clustering

Yeh, C.; Gu, Y.-Y.;

Computers and Digital Techniques, IEE Proceedings- , Volume: 142 Issue: 6 ,
Nov. 1995

Page(s): 401 -406

[\[Abstract\]](#) [\[PDF Full-Text \(592 KB\)\]](#) **IEEE JNL**

85 Hierarchical mapping of spot defects to catastrophic faults-design and applications

Gaitonde, D.D.; Walker, D.M.H.;

Semiconductor Manufacturing, IEEE Transactions on , Volume: 8 Issue: 2 , May
1995

Page(s): 167 -177

[\[Abstract\]](#) [\[PDF Full-Text \(1080 KB\)\]](#) **IEEE JNL**

86 Synchronous techniques for timing recovery in BISDN

Lau, R.C.; Fleischer, P.E.;

Communications, IEEE Transactions on , Volume: 43 Issue: 234 ,
Feb./March/April 1995

Page(s): 1810 -1818

[\[Abstract\]](#) [\[PDF Full-Text \(800 KB\)\]](#) **IEEE JNL**

87 Efficient and effective placement for very large circuits

Wern-Jieh Sun; Sechen, C.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
, Volume: 14 Issue: 3 , March 1995

Page(s): 349 -359

[\[Abstract\]](#) [\[PDF Full-Text \(980 KB\)\]](#) **IEEE JNL**

88 Active timing multilevel fault-simulation with switch-level accuracy

Meyer, W.; Camposano, R.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
, Volume: 14 Issue: 10 , Oct. 1995

Page(s): 1241 -1256

[\[Abstract\]](#) [\[PDF Full-Text \(1504 KB\)\]](#) **IEEE JNL**

89 Distributed hardwired barrier synchronization for scalable multiprocessor clusters

Shisheng Shang; Kai Hwang;

Parallel and Distributed Systems, IEEE Transactions on , Volume: 6 Issue: 6 ,
June 1995

Page(s): 591 -605

[\[Abstract\]](#) [\[PDF Full-Text \(1216 KB\)\]](#) **IEEE JNL**

90 Acute human testing of a dual chamber ventricular tachyarrhythmia detection algorithm at Mayo clinic

Brown, M.L.; Gillberg, J.M.; Stanton, M.S.; Hammill, S.C.; Olson, W.H.;
Computers in Cardiology 1996 , 8-11 Sept. 1996
Page(s): 61 -64

[\[Abstract\]](#) [\[PDF Full-Text \(380 KB\)\]](#) **IEEE CNF**

91 Modeling timed user-interactions in multimedia documents

Junehwa Song; Doganata, Y.N.; Kim, M.Y.; Tantawi, A.N.;
Multimedia Computing and Systems, 1996., Proceedings of the Third IEEE
International Conference on , 17-23 June 1996
Page(s): 407 -416

[\[Abstract\]](#) [\[PDF Full-Text \(776 KB\)\]](#) **IEEE CNF**

92 A flexible tool kit for the development of real-time applications

Ancilotti, P.; Buttazzo, G.; Di Natale, M.; Bizzarri, M.;
Real-Time Technology and Applications Symposium, 1996. Proceedings., 1996
IEEE , 10-12 June 1996
Page(s): 260 -262

[\[Abstract\]](#) [\[PDF Full-Text \(276 KB\)\]](#) **IEEE CNF**

93 DRTSS: a simulation framework for complex real-time systems

Storch, M.F.; Liu, J.W.-S.;
Real-Time Technology and Applications Symposium, 1996. Proceedings., 1996
IEEE , 10-12 June 1996
Page(s): 160 -169

[\[Abstract\]](#) [\[PDF Full-Text \(980 KB\)\]](#) **IEEE CNF**

94 Real-time emulation method for ATM switching systems in broadband ISDN

Matsumura, T.; Yamanaka, N.; Yamaguchi, R.; Ishikawa, K.;
Rapid System Prototyping, 1996. Proceedings., Seventh IEEE International
Workshop on , 19-21 June 1996
Page(s): 55 -60

[\[Abstract\]](#) [\[PDF Full-Text \(488 KB\)\]](#) **IEEE CNF**

95 Difference clocks: a new scheme for logical time in distributed systems

Vaidehi, S.; Ram, D.J.; Shukla, A.;

Computers and Digital Techniques, IEE Proceedings- , Volume: 143 Issue: 6 , Nov. 1996

Page(s): 426 -430

[\[Abstract\]](#) [\[PDF Full-Text \(536 KB\)\]](#) **IEEE JNL**

96 200-MHz superscalar RISC microprocessor

Vasseggi, N.; Yeager, K.; Sarto, E.; Seddighnezhad, M.;

Solid-State Circuits, IEEE Journal of , Volume: 31 Issue: 11 , Nov. 1996

Page(s): 1675 -1686

[\[Abstract\]](#) [\[PDF Full-Text \(1648 KB\)\]](#) **IEEE JNL**

97 Timing analysis speed-up using a hierarchical and a multimode approach

Blaquiere, Y.; Dagenais, M.; Savaria, Y.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 15 Issue: 2 , Feb. 1996

Page(s): 244 -255

[\[Abstract\]](#) [\[PDF Full-Text \(1152 KB\)\]](#) **IEEE JNL**

98 ChipEst-FPGA: a tool for chip level area and timing estimation of lookup table based FPGAs for high level applications

Min Xu; Kurdahi, F.J.;

Design Automation Conference 1997. Proceedings of the ASP-DAC '97. Asia and South Pacific , 28-31 Jan. 1997

Page(s): 435 -440

[\[Abstract\]](#) [\[PDF Full-Text \(668 KB\)\]](#) **IEEE CNF**

99 Proceedings of ASP-DAC '97: Asia and South Pacific Design Automation Conference

Design Automation Conference 1997. Proceedings of the ASP-DAC '97. Asia and South Pacific , 28-31 Jan. 1997

[\[Abstract\]](#) [\[PDF Full-Text \(548 KB\)\]](#) **IEEE CNF**

100 CB-Power: a hierarchical cell-based power characterization and estimation environment for static CMOS circuits

Wen-Zen Shen; Jiing-Yuan Lin; Jyh-Ming Lu;

Design Automation Conference 1997. Proceedings of the ASP-DAC '97. Asia and South Pacific , 28-31 Jan. 1997

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[\[Abstract\]](#) [\[PDF Full-Text \(524 KB\)\]](#) **IEEE CNF**

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101 Par-POPINS: a timing-driven parallel placement method with the Elmore delay model for row based VLSIs

Koide, T.; Ono, M.; Wakabayashi, S.; Nishimaru, Y.;

Design Automation Conference 1997. Proceedings of the ASP-DAC '97. Asia and South Pacific , 28-31 Jan. 1997

Page(s): 133 -140

[\[Abstract\]](#) [\[PDF Full-Text \(952 KB\)\]](#) **IEEE CNF**

102 Performance evaluation of a consensus algorithm with Petri nets

Segent, N.;

Petri Nets and Performance Models, 1997., Proceedings of the Seventh International Workshop on , 3-6 June 1997

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[\[Abstract\]](#) [\[PDF Full-Text \(924 KB\)\]](#) **IEEE CNF**

103 Synthesis support for design partitioning

Willoughby, J.;

Verilog HDL Conference, 1997., IEEE International , 31 March-2 April 1997

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[\[Abstract\]](#) [\[PDF Full-Text \(432 KB\)\]](#) **IEEE CNF**

104 A 2 ns access, 285 MHz, two-port cache macro using double global bit-line pairs

Osada, K.; Higuchi, H.; Ishibashi, K.; Hashimoto, N.; Shiozawa, K.;

Solid-State Circuits Conference, 1997. Digest of Technical Papers. 44th ISSCC., 1997 IEEE International , 6-8 Feb. 1997

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[\[Abstract\]](#) [\[PDF Full-Text \(1144 KB\)\]](#) **IEEE CNF**

105 Tools for documenting digital designs on the Web

Borriello, G.; Beal, D.; Tianyu Li;

Microelectronic Systems Education, 1997. MSE '97. Proceedings., 1997 IEEE International Conference on , 21-23 July 1997

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[\[Abstract\]](#) [\[PDF Full-Text \(208 KB\)\]](#) **IEEE CNF**

106 Fast volume rendering using adaptive block subdivision

Choong Hwan Lee; Kyu Ho Park;

Computer Graphics and Applications, 1997. Proceedings., The Fifth Pacific Conference on , 13-16 Oct. 1997

Page(s): 148 -157, 221

[\[Abstract\]](#) [\[PDF Full-Text \(1104 KB\)\]](#) **IEEE CNF**

107 Modulation classification via hierarchical agglomerative cluster analysis

Swami, A.; Sadler, B.;

Signal Processing Advances in Wireless Communications, 1997 First IEEE Signal Processing Workshop on , 16-18 April 1997

Page(s): 141 -144

[\[Abstract\]](#) [\[PDF Full-Text \(536 KB\)\]](#) **IEEE CNF**

108 Hashed and hierarchical timing wheels: efficient data structures for implementing a timer facility

Varghese, G.; Lauck, A.;

Networking, IEEE/ACM Transactions on , Volume: 5 Issue: 6 , Dec. 1997

Page(s): 824 -834

[\[Abstract\]](#) [\[PDF Full-Text \(160 KB\)\]](#) **IEEE JNL**

109 IEE Colloquium on Systems Engineering of Aerospace Projects (Digest No.1998/249)

Systems Engineering of Aerospace Projects (Digest No. 1998/249), IEE Colloquium on , 28 April 1998

[\[Abstract\]](#) [\[PDF Full-Text \(44 KB\)\]](#) **IEE CNF**

110 Hierarchical functional timing analysis

Kukimoto, Y.; Brayton, R.K.;

Design Automation Conference, 1998. Proceedings , 15-19 June 1998

Page(s): 580 -585

[\[Abstract\]](#) [\[PDF Full-Text \(632 KB\)\]](#) **IEEE CNF**

111 Adaptive synchronization*Ginosar, R.; Kol, R.;*

Computer Design: VLSI in Computers and Processors, 1998. ICCD '98.

Proceedings., International Conference on , 5-7 Oct. 1998

Page(s): 188 -189

[\[Abstract\]](#) [\[PDF Full-Text \(168 KB\)\]](#) **IEEE CNF**

112 A worst case timing analysis technique for optimized programs*Sung-Soo Lim; Jihong Kim; Sang Lyul Min;*

Real-Time Computing Systems and Applications, 1998. Proceedings. Fifth

International Conference on , 27-29 Oct. 1998

Page(s): 151 -157

[\[Abstract\]](#) [\[PDF Full-Text \(64 KB\)\]](#) **IEEE CNF**

113 Hierarchical design method for real-time distributed systems*Yamane, S.;*

Real-Time Computing Systems and Applications, 1998. Proceedings. Fifth

International Conference on , 27-29 Oct. 1998

Page(s): 189 -192

[\[Abstract\]](#) [\[PDF Full-Text \(740 KB\)\]](#) **IEEE CNF**

114 A worst case timing analysis technique for multiple-issue machines*Sung-Soo Lim; Jung Hee Han; Jihong Kim; Sang Lyul Min;*

Real-Time Systems Symposium, 1998. Proceedings., The 19th IEEE , 2-4 Dec.

1998

Page(s): 334 -345

[\[Abstract\]](#) [\[PDF Full-Text \(228 KB\)\]](#) **IEEE CNF**

115 Analyzing non-deterministic real-time systems with (max,+) algebra*Brat, G.P.; Garg, V.K.;*

Real-Time Systems Symposium, 1998. Proceedings., The 19th IEEE , 2-4 Dec.

1998

Page(s): 210 -219

[\[Abstract\]](#) [\[PDF Full-Text \(172 KB\)\]](#) **IEEE CNF**

116 Hierarchical architecture for real time causal delivery*Abouaissa, A.; Benslimane, A.;*

Local Computer Networks, 1998. LCN '98. Proceedings., 23rd Annual Conference

on , 11-14 Oct. 1998

Page(s): 374 -383

[\[Abstract\]](#) [\[PDF Full-Text \(1696 KB\)\]](#) [IEEE CNF](#)

117 FPGA mapping of sequential circuits with retiming

Jun-Yong Lee; Shragowitz, E.;

Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on , Volume: 6 , 31 May-3 June 1998

Page(s): 426 -429 vol.6

[\[Abstract\]](#) [\[PDF Full-Text \(388 KB\)\]](#) [IEEE CNF](#)

118 GateMaker: a transistor to gate level model extractor for simulation, automatic test pattern generation and verification

Kundu, S.;

Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998

Page(s): 372 -381

[\[Abstract\]](#) [\[PDF Full-Text \(768 KB\)\]](#) [IEEE CNF](#)

119 Diagnosis and characterization of timing-related defects by time-dependent light emission

Knebel, D.; Sanda, P.; McManus, M.; Kash, J.A.; Tsang, J.C.; Vallett, D.;

Huisman, L.; Nigh, P.; Rizzolo, R.; Peilin Song; Motika, F.;

Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998

Page(s): 733 -739

[\[Abstract\]](#) [\[PDF Full-Text \(588 KB\)\]](#) [IEEE CNF](#)

120 A test pattern generation algorithm exploiting behavioral information

Chiusano, S.; Corno, F.; Prinetto, P.;

Test Symposium, 1998. ATS '98. Proceedings. Seventh Asian , 2-4 Dec. 1998

Page(s): 480 -485

[\[Abstract\]](#) [\[PDF Full-Text \(96 KB\)\]](#) [IEEE CNF](#)

121 S-CFG: a representation model for system synthesis

Curatelli, F.; Mangeruca, L.; Chirico, M.;

Signals, Systems, and Electronics, 1998. ISSSE 98. 1998 URSI International Symposium on , 29 Sept.-2 Oct. 1998

Page(s): 326 -331

[\[Abstract\]](#) [\[PDF Full-Text \(476 KB\)\]](#) [IEEE CNF](#)

122 CHDStd-a model for deep submicron design tools

Cottrell, D.; Mallis, D.; Morrell, J.;

Design Automation Conference 1998. Proceedings of the ASP-DAC '98. Asia and South Pacific , 10-13 Feb. 1998

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[\[Abstract\]](#) [\[PDF Full-Text \(772 KB\)\]](#) **IEEE CNF**

123 FARA-a framework for adaptive resource allocation in complex real-time systems

Rosu, D.; Schwan, K.; Yalamanchili, S.;

Real-Time Technology and Applications Symposium, 1998. Proceedings. Fourth IEEE , 3-5 June 1998

Page(s): 79 -84

[\[Abstract\]](#) [\[PDF Full-Text \(148 KB\)\]](#) **IEEE CNF**

124 Hierarchy-a CHDStd tool for the coming deep submicron complex design crisis

Grout, S.; Ledenbach, G.; Bushroe, R.G.; Fisher, P.; Cottrell, D.; Mallis, D.;

DasGupta, S.; Morrell, J.; Sayah, J.; Gupta, R.; Patel, P.T.; Adams, P.;

Design Automation Conference 1998. Proceedings of the ASP-DAC '98. Asia and South Pacific , 10-13 Feb. 1998

Page(s): 257 -260

[\[Abstract\]](#) [\[PDF Full-Text \(444 KB\)\]](#) **IEEE CNF**

125 HiPART: a new hierarchical semi-interactive HW-/SW partitioning approach with fast debugging for real-time embedded systems

Hollstein, T.; Becker, J.; Kirschbaum, A.; Glesner, M.;

Hardware/Software Codesign, 1998. (CODES/CASHE '98) Proceedings of the Sixth International Workshop on , 15-18 March 1998

Page(s): 29 -33

[\[Abstract\]](#) [\[PDF Full-Text \(116 KB\)\]](#) **IEEE CNF**

126 Proceedings 1998 International Conference on Application of Concurrency to System Design

Application of Concurrency to System Design, 1998. Proceedings., 1998

International Conference on , 23-26 March 1998

[\[Abstract\]](#) [\[PDF Full-Text \(224 KB\)\]](#) **IEEE CNF**

127 The performance of the consensus algorithm running on FDDI

Sergent, N.;

Parallel and Distributed Processing, 1998. PDP '98. Proceedings of the Sixth Euromicro Workshop on , 21-23 Jan. 1998

Page(s): 77 -83

[\[Abstract\]](#) [\[PDF Full-Text \(748 KB\)\]](#) **IEEE CNF**

128 Using cone structures for circuit partitioning into FPGA packages*Brasen, D.R.; Saucier, G.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 17 Issue: 7 , July 1998

Page(s): 592 -600

[\[Abstract\]](#) [\[PDF Full-Text \(352 KB\)\]](#) **IEEE JNL****129 Performance evaluation of cell discarding mechanisms for the distribution of VBR MPEG-2 video over ATM networks***Cuenca, P.; Garrido, A.; Quiles, F.; Orozco-Barbosa, L.;*

Broadcasting, IEEE Transactions on , Volume: 44 Issue: 2 , June 1998

Page(s): 206 -215

[\[Abstract\]](#) [\[PDF Full-Text \(908 KB\)\]](#) **IEEE JNL****130 An improved lattice vector quantization scheme for wavelet compression***Knipe, J.; Xiaobo Li; Bin Han;*

Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on] , Volume: 46 Issue: 1 , Jan. 1998

Page(s): 239 -243

[\[Abstract\]](#) [\[PDF Full-Text \(124 KB\)\]](#) **IEEE JNL****131 Synthesis of checker EFSMs from timing diagram specifications***Ogoubi, E.K.; Cerny, E.;*

Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on , Volume: 1 , 30 May-2 June 1999

Page(s): 13 -18 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(440 KB\)\]](#) **IEEE CNF****132 Interaction among cost functions in placement***Sarrafzadeh, M.; Maogang Wang;*

VLSI and CAD, 1999. ICVC '99. 6th International Conference on , 26-27 Oct. 1999

Page(s): 32 -36

[\[Abstract\]](#) [\[PDF Full-Text \(436 KB\)\]](#) **IEEE CNF****133 Hierarchical scheduling of periodic messages in open system***Zhang, L.Y.; Liu, J.W.S.; Deng, Z.; Philp, I.;*

Real-Time Systems Symposium, 1999. Proceedings. The 20th IEEE , 1-3 Dec. 1999

Page(s): 350 -359

[\[Abstract\]](#) [\[PDF Full-Text \(272 KB\)\]](#) [IEEE CNF](#)

134 CubicWare: a hierarchical design system for deep submicron ASIC
Myung-Soo Jang; Hoon-Sang Jin; Byoung-Hyun Lee; Jin-Yong Lee; Seong-Jin Song; Taek-Soo Kim; Jeong-Taek Kong;
ASIC/SOC Conference, 1999. Proceedings. Twelfth Annual IEEE International ,
15-18 Sept. 1999
Page(s): 168 -172

[\[Abstract\]](#) [\[PDF Full-Text \(344 KB\)\]](#) [IEEE CNF](#)

135 Challenges in clockgating for a low power ASIC methodology
Garrett, D.; Stan, M.; Dean, A.;
Low Power Electronics and Design, 1999. Proceedings. 1999 International
Symposium on , 16-17 Aug. 1999
Page(s): 176 -181

[\[Abstract\]](#) [\[PDF Full-Text \(376 KB\)\]](#) [IEEE CNF](#)

136 A timing verifier and timing profiler for asynchronous circuits
Karlsen, P.A.; Roine, P.T.;
Advanced Research in Asynchronous Circuits and Systems, 1999. Proceedings.,
Fifth International Symposium on , 19-21 April 1999
Page(s): 13 -23

[\[Abstract\]](#) [\[PDF Full-Text \(116 KB\)\]](#) [IEEE CNF](#)

137 A recursive PVM implementation of an image segmentation algorithm with performance results comparing the HIVE and the Cray T3E
Tilton, J.C.;
Frontiers of Massively Parallel Computation, 1999. Frontiers '99. The Seventh
Symposium on the , 21-25 Feb. 1999
Page(s): 146 -153

[\[Abstract\]](#) [\[PDF Full-Text \(44 KB\)\]](#) [IEEE CNF](#)

138 A hierarchical traffic shaper for packet switches
Surong Zeng; Uzun, N.;
Global Telecommunications Conference, 1999. GLOBECOM '99 , Volume: 2 , 1999
Page(s): 1655 -1659 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(432 KB\)\]](#) [IEEE CNF](#)

139 An 18-Mb, 12.3-GB/s CMOS pipeline-burst cache SRAM with 1.54 Gb/s/pin
Cangsang Zhao; Bhattacharya, U.; Denham, M.; Kolonsek, J.; Lu, Y.; Yong-Gee Ng; Nintunze, N.; Sarkez, K.; Varadarajan, H.D.;
Solid-State Circuits, IEEE Journal of , Volume: 34 Issue: 11 , Nov. 1999

Page(s): 1564 -1570

[\[Abstract\]](#) [\[PDF Full-Text \(508 KB\)\]](#) **IEEE JNL**

140 Harmony: static noise analysis of deep submicron digital integrated circuits

Shepard, K.L.; Narayanan, V.; Rose, R.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 18 Issue: 8 , Aug. 1999

Page(s): 1132 -1150

[\[Abstract\]](#) [\[PDF Full-Text \(404 KB\)\]](#) **IEEE JNL**

141 High-level synthesis of power-optimized and area-optimized circuits from hierarchical data-flow intensive behaviors

Lakshminarayana, G.; Jha, N.K.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 18 Issue: 3 , March 1999

Page(s): 265 -281

[\[Abstract\]](#) [\[PDF Full-Text \(388 KB\)\]](#) **IEEE JNL**

142 A hierarchical based approach for coupling aware delay analysis of combinational logic blocks

Ninglong Lu; Hajj, I.N.;

Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on , Volume: 2 , 17-20 Dec. 2000

Page(s): 1012 -1015 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(308 KB\)\]](#) **IEEE CNF**

143 Fast hierarchical floorplanning with congestion and timing control

Ranjan, A.; Bazargan, K.; Sarrafzadeh, M.;

Computer Design, 2000. Proceedings. 2000 International Conference on , 17-20 Sept. 2000

Page(s): 357 -362

[\[Abstract\]](#) [\[PDF Full-Text \(952 KB\)\]](#) **IEEE CNF**

144 Application-based, transistor-level full-chip power analysis for 700 MHz PowerPC™ microprocessor

Cheng, Y.-K.; Bearden, D.; Suryadevara, K.;

Computer Design, 2000. Proceedings. 2000 International Conference on , 17-20 Sept. 2000

Page(s): 215 -220

[\[Abstract\]](#) [\[PDF Full-Text \(556 KB\)\]](#) **IEEE CNF**

145 Resource scheduling in dependable integrated modular avionics*Yann-Hang Lee; Daeyoung Kim; Younis, M.; Zhou, J.; McElroy, J.;*

Dependable Systems and Networks, 2000. DSN 2000. Proceedings International Conference on , 25-28 June 2000

Page(s): 14 -23

[\[Abstract\]](#) [\[PDF Full-Text \(328 KB\)\]](#) **IEEE CNF**

146 Multilevel optimization for large-scale circuit placement*Chan, T.F.; Cong, J.; Tianming Kong; Shinnerl, J.R.;*

Computer Aided Design, 2000. ICCAD-2000. IEEE/ACM International Conference on , 5-9 Nov. 2000

Page(s): 171 -176

[\[Abstract\]](#) [\[PDF Full-Text \(612 KB\)\]](#) **IEEE CNF**

147 A timing-constrained algorithm for simultaneous global routing of multiple nets*Jiang Hu; Sapatnekar, S.S.;*

Computer Aided Design, 2000. ICCAD-2000. IEEE/ACM International Conference on , 5-9 Nov. 2000

Page(s): 99 -103

[\[Abstract\]](#) [\[PDF Full-Text \(580 KB\)\]](#) **IEEE CNF**

148 2-D object recognition by structured neural networks in a pyramidal architecture*Cantoni, V.; Petrosino, A.;*

Computer Architectures for Machine Perception, 2000. Proceedings. Fifth IEEE International Workshop on , 11-13 Sept. 2000

Page(s): 81 -86

[\[Abstract\]](#) [\[PDF Full-Text \(428 KB\)\]](#) **IEEE CNF**

149 Statistical timing macromodels of digital IP libraries*Zanella, S.; Neviani, A.; Franzimi, B.; Guardiani, C.;*

Statistical Metrology, 2000 5th International Workshop on , 11 June 2000

Page(s): 76 -79

[\[Abstract\]](#) [\[PDF Full-Text \(480 KB\)\]](#) **IEEE CNF**

150 Parasitic extraction for multimillion-transistor integrated circuits: methodology and design experience*You, E.; Swee Yew Choe; Chin Kim; Varadadesikan, L.; Aingaran, K.; MacDonald, J.;*

Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000 , 21-24 May 2000

Page(s): 491 -494

[\[Abstract\]](#) [\[PDF Full-Text \(368 KB\)\]](#) **IEEE CNF**

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